Digital Logic Analyser Help Index

This is the table of contents for the help system. Instructions on how to use the help system are also available.

File Menu

The File Menu includes commands that enable you to open, save and create sample files. It also allows you to print the current sample file.

For more information on any of these topics select one of the file menu commands shown below:

New	Create a new sample file.
Open	Open an existing sample file.
Save	Save the current sample to file.
Save As	Save the current sample to another file.
Print	Print the current sample file.
Exit	Exit Digital Logic Analyser.

Edit Menu

The Edit Menu includes commands that enable you edit the channel display settings, edit the trigger value, edit the hardware address and edit the display colours.

For more information on any of these topics, select one of the edit menu commands shown below:

Labels	Edit label description and settings.
Trigger	Edit hardware trigger settings.
Hardware	Edit hardware address.
Description	Edit sample description.
Colours	Edit display colours.

Search Menu

The Search Menu includes commands that enable you to search the current sample data for a specific sample value.

For more information on any of these topics, select one of the Search menu commands shown below:

Search	Set data search criteria.
Next	Find next search data.
Previous	Find previous search data.
Trigger Search	Find trigger data.

Help Menu

The Help Menu provides commands that enable you to get help on the different aspects of the system. If you require more help on how to use the help system refer to the instructions on how to use the help system. The help menu provides the following help.

Using Help
This option provides help on how to use the help system. It is identical to selecting F1 from within the Windows help system.

Help On Keys
This option provides help on what keys perform what tasks within the Digital Logic Analyser software. This is identical to the Keyboard and Mouse help contained in the help index.

Help Index
This option presents the Digital Logic Analyser Help Index . From here more specific help is available by selecting from the topics presented.

Help Instructions

You can find information in the Help System by using the index or the search features provided. To return to the Help Index click on the Back button or press the B key. For complete instructions on how to use Help press the F1 key while the Help window is active. Help on using help is also available from the help menu above.

To use the Help Index
Select a topic from the index. This can be achieved by doing one of the following:

- Click on any underlined topic.
- Press the TAB key until the request topic is highlighted and then press the ENTER key.

To scroll in the Help window
Do one of the following:

- Use the up arrow or down arrow keys from the numeric keypad
- Click on the scroll bars up and down arrows.

To return to the previous topic

- Click the on Back button or press the B key.

To open the Search feature in Help

- Click the on Search button or press the S key.

To close the Help window

- From Help's File menu, choose Exit (ALT, F, X).

Help with Keyboard and Mouse Commands

This Digital Logic Analyser software allows full control using both the keyboard and mouse. Below is a description on the functionality assigned to the different mouse and keyboard actions.

Keyboard Commands
From the Digital Logic Analyser software main screen use the TAB key to move between the different control groups. The five groups, in order, are the data display screen, the sample frequency control, the time base setting and the hardware control buttons. More information on using the controls is given in control descriptions Once a control group has focus the left and right arrow keys on the numeric keypad provide selectivity within that group.

Accelerator Keys
The Digital Logic Analyser software makes full use of keyboard accelerators. All the major menu selections have a corresponding accelerator define. For example from the main screen typing Alt-x will invoke the exit action and is an accelerator for the File/Exit menu command. In addition, all the button controls have an accelerator defined. The character marked with the underscore represents the accelerator. For example the Start button can be pressed by selection the 'S' character from the keyboard.

Mouse Control
By using the mouse it is possible to select the action directly. To do so just requires selecting the control with the mouse pointer and clicking the left mouse button. More information on mouse functionality is given in control descriptions

Application Control Description

The Digital Logic Analyser main screen is made up of five controls. These are described in detail below.

Data Display Control
This control displays the sample data results. When selected the use of the arrow keys on the numeric keypad will scroll the data left or right. The same result can be achieved by clicking on the left or right arrows keys using the mouse. The mouse also allows auto scrolling. This can be achieved by holding down the left mouse button while within the data display window and moving the mouse to the left or right of the data display window, while keeping the left mouse button depressed. By double clicking the left mouse button from within the data display window the Edit Trigger dialog will be activated. By double clicking on the left mouse button from within the channel display the Edit Labels dialog will be activated.

To perform a ***frequency and period measurement***, just select an anchor point using the right mouse button and then select the end point using the shift key right mouse button combination. The result of the calculation is displayed in the frequency and period static text windows of the status bar.

Sample Frequency Control
This control allows you to select the required sample frequency. To change the sample frequency tab to the control until it has focus and use the '+' or '-' keys to spin the sample frequency value. The same result can be achieved by clicking on the up or down arrows with the mouse. This control is disabled if the system is running on an external sample clock.

External Frequency Control
If the hardware external frequency switch has been selected, the external frequency entry field is enabled. So that the software knows at what frequency the sample is running, it is up to the user to enter the correct external frequency. This control is disabled if the system is running on its internal sample clock.

Time base Controls
This control group selects the data display time base and controls how the data is to be displayed. There are four time base settings ranging from one to eight and each represents varying degrees of magnification. The timebase can be change by clicking on the required timebase using the mouse or by selecting the appropriate numerical key (ie 1,2,4 or 8).

Hardware Controls
The two hardware controls are Start and Abort. The Start will initiate a start sample procedure. Once started the system will keep sampling until triggered and at that point will automatically stop and display the results of the sample. If a trigger is not located it is possible to abort the sample using the Abort sample button. The current sample status is displayed in the status window.

File New Command

Use this command to create a new sample document. It will reset the current settings to their default values. Once a new sample file is created the current sample file is overwritten, so remember to save the current sample file if it is still required. This action also places the application in its demonstration mode.

File Open Command

Use this command to open an existing sample document. This command allows you to restore a previously saved sample document. The newly open sample file will overwrite the current sample file, so remember to save the current sample file if it is still required. The default file extension for the sample document is DLA.

File Save Command

Use this command to save the current sample document to a file. This allows a permanent record of the sample data to be made. The data, once saved can be recovered at a later date using the File Open command.

File Save As Command

Use this command to save the current sample document to a alternatively named sample document. This allows a permanent record of the sample data to be made. The data, once saved can be recovered at a later date using the File Open command.

File Print Command

Use this command to print the current sample data. The print command provides standard Windows 3.x print support. The printout consist of the currently displayed data, the sample descriptive text, the sample frequency and the sample file name. The print out maintains the currently selected timebase setting and this is reflected in the final the print out. Note that only the currently displayed data is printed and that the entire data set of sample results will not be printed on a single print output.

File Print Setup Command

Use this command to perform any print setup required. The print setup provides the standard Windows 3.x printer setup support. This menu option allows you to select the desired printer and configure the printer output options.

File Exit Command

Use this command to exit the Digital Logic Analyser. You can also end the application using the Windows task list or using the application system menu and selecting **Close**. Be warned that if the current sample document has not been saved the data will be lost.

Edit Labels Command

Use this command to change the channel label descriptions. This command presents a dialog box, allowing the individual channel labels to be altered. It also allows selective channels to be enabling or disabled. Any disabled channels will not be displayed.

This command can also be activated by double clicking the left mouse button within the channel display area.

The label information is part of the sample document and as such this information is automatically saved and restored as part of the sample document file.

Edit Trigger Command

Use this command to program the trigger control data. The digital logic analyser has a programmable trigger and triggering is controlled by the first four input channels (ie 1,2,3,4). This dialog box allows any of these four channels to trigger on a high, low or don't care state. All four channels must be triggered before the hardware will start sampling.

A high/low level requires the channel to be high/low respectively before that channel generates a trigger. A don't care removes that channel from the trigger mechanism. For example a high on channel 1 and don't care on the remaining three channels will result in the hardware triggering only when channel 1 goes high irrespective of the remaining 3 channels.

This command can also be activated by double clicking the left mouse button within the data display area.

Edit Description Command

Use this command to edit the descriptive text associated with the sample document.

This multi line entry field allows text up to the buffer length (approximately 300 bytes) to be added. The erase button will clear the current buffer contents. The cancel key allows you to abort the current edit operation.

The description information is part of the sample document and as such this information is automatically saved and restored as part of the sample document file.

Edit Hardware Command

Use this command to modify the digital logic analyser hardware I/O address. Be careful when setting this address, because if you select a I/O port that is already in use by the operating system or another piece of hardware the system may behave in an unpredictable manner or at worst may even ***crash.*** If you notice erratic or inconsistent sample data being generated, it is possible a port conflict may exist, so try a different hardware I/O address.

The address selected must match the dip switch settings of the interface card and the digital logic analyser unit. To test that the hardware is being correctly located by the software, toggle the internal/external clock switch on the front panel of the logic analyser. This change in clock source should be reflected in the Clock Status located at the bottom left of the screen. If no change is observed the software address does not match the hardware address so make the required adjustment and try again.

The recommended default setting is **0F30** in hex. If you are experiencing trouble it is recommended you try the address **0E30, 0D30, 0C30...** etc. For more information refer to a IO Map for the IBM XT and AT computers.

Note: the hardware address entry field will only accept input in hex format.

Edit Colours Command

Use this command to customise the data display colours. This option presents a dialog box allowing the data display background colour, line colour and line thickness to be modified.

The background colour can be either a solid colour or one of the grid line tiles. The line thickness can be set to thin or thick. Unless the user is running the software on a 486 machine or better, it is suggested, for performance reason, that the thin line setting should be selected.

Search Command

Use this command to search for a particular sample data. This command will present you with a dialog box that will allow you to specify the search criteria.

A channel can be marked as low, high or don't care. If the channel is mark high/low then the search will only consider that channel if the data matches the high/low state. A don't care removes the channel from influencing the search. All individual channel search criteria must be met before the search succeeds.

For example to search for the hex value 01H you would set all the channels to 0 except for channel #1 which would be set to 1. To search for all cases where the most significant bit is 0 you would set channel #8 to 0 and all the other channels to don't care (X).

If the search fails to find any data that matches the search criteria the system will generate a beep.

Search Next Command

Use this command to repeat the search against the current search criteria. This will search the display data in a forward direction.

If the search fails to find any data that matches the search criteria the system will generate a beep.

Search Previous Command

Use this command to repeat the search against the current search criteria. This will search the display data in the reverse direction.

If the search fails to find any data that matches the search criteria the system will generate a beep.

Search On Trigger Command

Use this command set the search criteria to match the sample trigger criteria and to perform a search against the current search criteria

If the search fails to find any data that matches the search criteria the system will generate a beep.

Digital Logic Analyser For Windows 3.0

Digital Logic Analyser for Windows 3.x

The Digital Logic Analyser for Windows transforms a standard PC into a fully functional hardware logic analyser, perfect for debugging those digital electronic circuits that you have been struggling to get to work.

The unit offers features including 8 input channels with a programmable trigger on 4 of the 8 input channels, a 2k sample buffer enabling long sample runs, an internally generated clock that produces a sample rate of 100kHz up to 6.00 MHz in steps of 100kHz and an external clock feature that allows sample rate to be increased up to and beyond the 10Mhz bandwidth. In addition to this, all channels have diode over voltage protection, which means the unit is suitable for not only TTL and HC digital signals, but also for higher voltage signals such as RS233. The hardware is controlled by an easy to use Windows based application that is packed full of features including printing, file handling, data searching and a full online help facility.

All this an more is provided in a very low cost kit ideal for the electronics enthusiast. Please note that although the quality of the PCB's supplied makes for simple construction, this kit does requires some ***electronics construction*** and as such it is only suitable for those with a ***basic knowledge*** of electronics and preferably some prior experience with electronic kit construction.

The Digital Logic Analyser for Windows was designed and developed by Jussi Jumppanen. The design and development of the hardware and the Windows 3.x software was carried out in cooperation with Xidicone Pty Ltd.

The product is sold in kit form a kit only. The kit consists of two high quality double sided plated through the printed circuit boards, the Windows 3.x software and a collection of some of the harder to get parts. The remaining parts will need to be sourced separately by the purchaser. These parts consist of a handful of stock standard 74HCXXX components and can be easily obtained at any electronics component supplier. The cost of these additional components will vary from $AUS40.00 to $AUS80.00 depending on the markup of the supplier. For more information or for details on ordering the product please refer to the ordering the product section.

Any product enquires should be address to Jussi Jumppanen

Jussi Jumppanen

Please send all enquires to:

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PO Box 697
Lanecove NSW 2066
Australia

Voice and E-mail details:

Telephone: 061-02-428 3927 (H)
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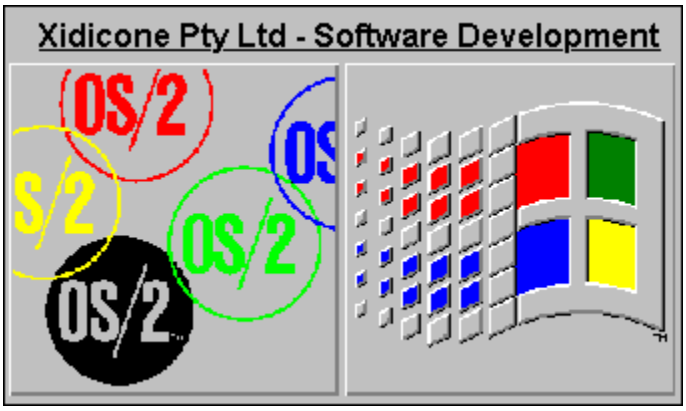
Compuserve: 100352,1572



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Clipboard

ic that describes the term "clipboard". The word "clipboard" is underlined in the Copying Text and Glossary topics to indicate that it is a help term for which a pop-up explanation is available. If you click the "clipboard" term This is a topwithin the Copying Text or Glossary topic, this help topic will be displayed in a pop-up window.
(This topic is also tagged with the keyboard "clipboard", for use with the WinHelp search option.)

Sample Data

IO Map for IBM XT and AT

Below is a list of the IO mapping for the AT and XT machines. The list is given ***as is*** without warranty of any kind. All care has been taken to ensure that the contents of this table are correct, but the contents are in no way guaranteed.

Address	Usage	Used on AT	Used on XT
000-00F	First DMA Controller	used	used
010-01F	Expansion Adaptor	available	available
020-021	First Interrupt Controller	used	used
022-03F	Reserved	-	-
040-047	Timer/Counter	used	used
048-05F	Reserved	-	-
060-064	8255 (or 8042)	used	used
070-071	Real Time Clock	used	available
072-07F	Reserved	-	-
080-08F	DMA Registers	used	used
090-09F	Reserved	-	-
0A0-0A1	NMI Registers	used	used
0A2-0BF	Reserved	-	-
0C0-0CF	Second DMA Controller	used	available
0D0-0DF	Reserved	-	-
0E0-0EF	Free	available	available
0F0-0FF	80287 (80387)	used	used
100-1EF	Free	available	available
1F0-1FF	AT H/D Controller	used	available

Address	Usage	Used on AT	Used on XT
200-207	Games Port	used	used
208-20F	Free	available	available
210-21F	XT expansion	available	used
278-2F7	Second Printer port	used	used
2E0-2EF	Free	available	available
280-20F	Free	available	available
2B0-2DF	1. EGA adaptor 2. IBM 3270 Emulation card	used	used
2E0-2EF	Free	used	used
2F0-2F7	Reserved	-	-
2F8-2FF	Second RS-232c port	used	used
300-31F	free	available	available
320-32F	H/D Controller for XT	available	used
330-36F	Free	available	available
370-377	Reserved	used	used
378-38F	SDLC adaptor	used	used

390-3AF	Free	available	available
3B0-3BB	Reserved	-	-
3BC-3BF	Monochrome Display	used	used
3C0-3CF	EGA or VGA	used	used
3D0-3EF	CGA	used	used
3E0-3EF	Free	available	available
3F0-3F7	F/D controller	used	used
3F8-3FF	First RS-232c port	used	used

NOTE: The Digital Logic Analyser requires a full 256 sequential IO slots. This is a design feature to allow future chaining of other such devices. For this reason the free area as shown above is generally ***not*** suitable for use for the logic analyser hardware address. It is suggested you use IO locations above the last reserved location (ie **0F30** is the recommended address).

Digital Logic Analyser for Windows 3.x Order Form

Postal Address: **Xidicone Pty Ltd**
PO BOX 697
Lanecove NSW 2066
Australia

Placing and order: To place and order print this form by clicking on the Print Topic in the File pull-down menu. Make sure the printer is setup for portrait mode

Ordering by Check or Money Order: To order by check or money order, fill in the order form, and send it along with a check made out to Xidicone Pty Ltd, to the address indicated above. **Payments must be in Australian dollars drawn on a Australian Bank.**

Ordering by Credit Card: To order by credit card, fill in the order form and relevant credit card details and send the details to Xidicone Pty Ltd at the postal address indicated above. **Please note the credit card will debited and amount equivalent to the price listed in Australian dollars.**

The Digital Logic Analyser for Windows 3.x Kit includes the following:

- IBM XT I/O Card PCB and Digital Logic Analyser PCB
- Digital Logic Analyser for Windows 3.x Software (latest version)
- Complete set of build instructions.
- Hard to get parts: 2.00 Mhz XTAL, 74HC4046, 74HC688, 74HC4040, 6116/100

Note: The kit supplied does not contain a complete set of parts. Some additional IC's nad other parts will need to be purchased seperately in order to complete the kit.

The source code for the software is also available. To compile the source code requires the Borland C++ 3.1 compiler, the Borland OWL Version 1.0 and the Windows 3.x SDK.

Postage will be by airmail. The listed price is guarantied through to December 1994. All prices quoted are in Australian dollars only.

```
Please supply me: with quantity ___ kit(s) @ $AUS 130.00 each  = ___________
            with/without source code       @ $AUS  85.00       = ___________
            including post and handling    @ $AUS  15.00       =       15.00
                                            Total Payment: $AUS  ___________

       Name: _____________________________________   Date: _____________
    Company: ____________________________________________________________
    Address: ____________________________________________________________
             ____________________________________________________________
City, State: _____________________________     Zip: ____________________
    Country: _____________________________
 Media Size: 5.25" Disk ____ or 3.5" Disk ____ or Either size ____
```

Credit Card Details

```
Card holders Name:  ____________________________________________
        Card Type:  Mastercard ___       Visa ___       Bankcard ___
      Card Number: |__|__|__|__| |__|__|__|__| |__|__|__|__| |__|__|__|__|
       Card Valid: ____ / ____  to  ____ / ____
Phone Number: (____)___________________
```

Signature: _____

Important Note:

All remittance will be in Australian Dollars ($AUS) only, based on the exchange rate at the time of purchase. Consult the current exchange rate for the approximate cost in other currencies.

Debug Dialog Box

To enable the hardware debugging option you need to add **-DEBUG** to the program argument list. This can be done by highlighting the DLA program icon and selecting the File/Properties menu option from the Windows Program Manager (see your Windows User Guide for further details).

Once enabled the debug option adds the Debug menu item to the standard menu. By selecting this menu item you will be presented with the Hardware Debug dialog box. For help on debugging refer to the hardware debugging tips section.

The dialog box provides the following functionality:

Start Button
This lets you start the sample using the current dialog box settings

Abort Button
This lets you abort the current sample.

Sample Frequency
This option lets you set the hardware sample frequency in real time. As the frequency is adjusted the hardware frequency generation circuit will adjust accordingly.

Run Mode
This option lets you run the hardware in the normal run mode or a special debug run mode. In debug mode the hardware will enable the RAM and address generation circuits. It does this by raising the ALWAYS signal high.

Trigger Mode
This option lets you set the trigger mode to always trigger meaning the trigger hardware is always guarantied to generate a trigger signal or setting the trigger mode to never meaning the trigger hardware will never generate a trigger signal. In this mode the hardware must be aborted.

Hardware Debugging Tips

This section on debugging the hardware assumes you have access to an oscilloscope (CRO).

Overview of Hardware
The hardware consists of four major regions, these being the clock generation circuit, the ram and address circuit, the trigger circuit and the hardware control circuit. Of these different areas the two that are most likely to cause problems is the clock generation and the ram and addressing. The debug dialog is designed to help with the debugging of these parts of the hardware.

Clock Generation Testing
For the clock circuit to work as designed requires a fairly noise free environment and a good base clock. The dialog box provides a frequency spin button that allows the frequency to be adjusted from 100 kHz to 6.0 MHz in steps of 100 kHz. If the CRO channel lead is attached to the sample clock test point (SCLK) and the spin button is moved from 100 kHz to 6.0 MHz in steps of 100 kHz the CRO should also register a clean wave form of the same frequency over the entire range.

If it fails to do so the first point to check is **Pin 8 of IC15** which should be running at 2.00 MHz. If this clock is not running the chip is either damage or the circuit is not self starting. To test for the self starting problem man handle the crystal in an effort to get it to start.

The next point to test is **Pin 5 of IC12.** This point should be running a clean square wave at 100 kHz. If it is not check the **Pin 13 of IC19** which should be running at 200 kHz. A point of interest is that IC19 is like all clocked devices and is susceptible to slow rise time sources. For the IC19 to operate correctly the input clock needs to have a fast rise time and it turns out that the 74HC04 does not produce a clock with a suitably high rise time. It is for this reason IC15 is designated as a 74LS04 and not a 74HC04 device. The 74HC04 is definitely not suitable as the clock source.

The last part of the clock generation circuit is IC13, IC20 and IC21. For this circuit to be functioning properly the clock source at Pin 14 of IC13 will match the feedback clock at Pin 3 of IC13. If this is not the case check the two counters IC20 and IC21 for correct operation.

Ram Addressing Test
To test the ram addressing circuit a suitable sample frequency needs to be selected, the run mode should be set to ***run debug*** and the trigger mode set to ***never trigger.*** In this configuration the hardware will never trigger (so it will run indefinitely) and the address circuit will be enabled meaning the ram circuit will be continually writing the input data to RAM. In this mode it is possible to check that the address generation circuits of **IC7, IC8** and **IC9** are working and that the RAM circuit **IC10** is working correctly.

Data Display Mode

This menu option allows you to change the way the data is displayed. The data can be displayed in the default graphical format or it can alternatively be displayed as raw hex data in a listbox configuration.

In this listbox display mode the search functionality is still provided but as printing is not supported, the print menu option is disabled. In addition the colours and the channel labels don't have any meaning so these menu options are also disabled.